IN THE SPECIFICATION:

Please amend page 3, fourth full paragraph as follows:

Here, when a large size panel is used, a load applied to per source signal line is increased. In order to reduce the influence of rounding of a signal due to the load, a signal amplifying circuit is required. Thus, in the block diagram shown in Fig. 10, the analog buffer circuits (AB.1 to AB.x) 109 are located as signal amplifying circuits before the signals are outputted to the source signal lines. An example of the analog buffer circuit is shown in Fig. 5.

IN THE DRAWINGS:

Applicants hereby corrects Figures 5-7 by replacing "Prior" with --Prior Art--.

REMARKS

The Office Action of December 27, 2002 was received and carefully reviewed. Reconsideration and withdrawal of the currently pending rejections are requested for the reasons advanced in detail below.

Filed concurrently herewith is a *Request for a Two Month Extension of Time* which extends the shortened statutory period of response to May 27, 2003. Accordingly, Applicants respectfully submit that this response is being timely filed.

Claims 1-28 were pending prior to the instant amendment. By this amendment Applicants cancel claims 7-14 without prejudice to file a divisional application directed thereto. Consequently, claims 1-6 and 15-28 are currently pending in the instant application.

Initially, addressing the Office Action, Figures 5-10, 15 and 18 are objected to for failing to include the legend "Prior Art" thereon. Figures 5, 6, and 7 are amended herein to include the "Prior Art" legend to overcome this objection. With regard to Figures 8-10, 15 and 18, Applicants have not confirmed whether these figures should include such a legend. As a result, these figures are not amended at this time.